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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,776	01/12/2004	Bruce Archambeault	FIS920030309	1775

29505 7590 06/07/2007

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EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
06/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/707,776	ARCHAMBEAULT ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *31-38* is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/707,776 filed on 4/9/2007.

Claims 1-38 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10, 12-14 and 16-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Frank et al. (6,907,589 B2).

4. As to claims 1 and 23, Frank et al. teach system and method for evaluating vias per pad in a package design (Fig. 4-8). The system comprises a graphical user interface for displaying design rule violations from design rule checker software (DRC) (Fig. 4). The method for evaluation of design rule violations as taught by Frank et al. using that system comprising graphically displaying the output from text of design tool (DRC) (col. 6 lines 10-20); graphically listing design rule violations (col. 6; Fig. 4-5; Fig. 5 shown graphically listing of design rule violations; col. 9 describes design rule checks list); displaying said output as part of a software layer of said design tool (CAD software and DRC software) such that no permanent changes are made to any original design file (Fig. 5 shown displaying design rule violations); generating and annotating a subset

output file (part of design rules) for use by other users (Fig. 5; col. 6); and generating software help functions allowing said user to gain information about design rule violations (CAD software has capability of perform such functions). Note that the system as taught by Frank et al. can be used by a group of designers (users) as team. Therefore multiple users can gain access and information as well by the system. Since the system as taught by Frank et al. is for evaluating design rule checking for violations of an electronic design, therefore such original design file must be preserved (no permanent changes should be made). In addition, Frank et al. also displaying graphical and textual representation of design rule violations of an electronic design having a multiple layers (see abstract, Fig. 4 and its description).

5. As to claim 2, Frank et al. teach design tool is a design rule checking system (Fig. 4, DRC, evaluation software and CAD software).

6. As to claims 3 and 24, Frank et al. teach said text comprises text output from said design tool (col. 6 lines 10-58).

7. As to claims 4 and 25, Frank et al. teach said text output from said design tool comprising an input file (design database of electronic design) for software implementing said method (Fig. 4, design database).

8. As to claims 5 and 26, Frank et al. teach plural of design rules (Fig. 4) that can be selected by an individual designer (user) for design rule checking software.

9. As to claims 6, 21 and 27, Frank et al. teach a system that includes design rule checking software including evaluating software to evaluate via per pad rules (Fig. 4; software layer of design tool). Since the output from design rule checking is report;

such report can be deleted when no longer required or needed in order to save memory.

10. As to claims 7, 22 and 28, Frank et al. design rule checking software including CAD software. Therefore, such software must include a pop-up window display for facilitating design rule checking.

11. As to claim 8, Frank et al. design rule checking software including CAD software. Therefore, such software must include a pop-up window display for facilitating design rule checking. Fig. 5 shows displaying design rule violations of an electronic design including information identifying said design rule violations (vias per pad rules; traces rules), net name (traces), component name and information relating to design rules (Fig. 8; col. 5).

12. As to claim 9, Frank et al. teach design rule checking for violations including identification of parameters being checked along with information as to the parameter's importance (vias per pad, net checking, traces checking described as example in col. 5-6; see also description of Fig. 4, 7 and 8 for various design rule checking).

13. As to claim 10, Frank et al. design rule checking software including CAD software that has capability of drawing a bounding box around any of design rule violations.

14. As to claim 12, Frank et al. report (subset of file) summarizing via per pad violations (Fig. 4) that can be saved.

15. As to claim 13, Frank et al. design rule checking system (Fig. 4) for use to check various design rule violations of an electronic design including reporting summary of

design rule violations. Since the information of design rule violations is important for all designers, such information must be saved for sharing purpose with different users.

16. As to claim 14, Frank et al. design rule checking system (Fig. 4) for use to check various design rule violations of an electronic design including reporting summary of design rule violations. Since the information of design rule violations is important for all designers, such information must be saved for sharing purpose with different users. In order to save memory space, only the information requested by user must be saved and the original design file must be kept as historical data.

17. As to claim 16, Frank et al. teach various design rules that can be used or selected for design rule checking software and CAD software (Fig. 4). The software tool as taught by Frank et al. must include reselection mode option to return an originally presented view for facilitating design rule checking.

18. As to claims 17 and 29, remarks set forth in rejection of claims 1 and 23 equally applied in rejecting claims 17 and 29. Frank et al. reporting summary of design rule violations from design rule checking software, where the report of violations can be viewed in a display unit (Fig. 4). Frank et al. teach design database of an electronic circuit design (Fig. 4). Frank et al. also teach generating a subset output file (report of different design rule violations) (Fig. 4, 7, 8). Frank et al. also teach editing said design file (input design file) based on said violations (Fig. 8).

19. As to claim 18, Frank et al. teach inputting design data (Fig. 4, 6, 8, design database, input design); and rule checker parameters into design rule checking tool (Fig. 4, 6, 8) and performing design rule checking (Fig. 4, 6, 8).

20. As to claims 19 and 30, Frank et al. teach reporting design rule violations (textual file) (Fig. 4, 8).

21. As to claim 20, Frank et al. teach a system and method for design rule checking for various design rule violations of an electronic circuit design. Thus, each of design rule violation can be selected and used by individual user among designers.

Allowable Subject Matter

22. Claims 11 and 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if rewritten or amended to overcome the claim objections set forth in this Office action. The prior art of record does not teach or fairly suggest loading and viewing said subset output file without running said design tool rule checker and the software help functions as recited in the claim.

23. Claims 31-38 are allowed over the prior art of record.

Remarks

24. Applicants argued that Frank described only textual representation of design rule violation. It is not true. Frank teaches both graphically representation and textual representation of design rule violations as indicators of design rule violations (at least see abstract and Fig. 4). Any portion of design rule violations of multiple layers of an electronic design can be graphically and/or textual displayed for a user or circuit designer to make necessary design rule correction to meet design rule requirements. Thus, Frank does not only displaying a text report of design rule violations of a multiple layers of an electronic design to a designer or user, but Frank also displaying graphical

representation of design rule violations. In addition, Frank does not teach there are permanent changes made to any original design file.

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, AU: 2825